IN THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1.-29. (Cancelled).

30. (New) A memory system comprising:

a plurality of central units, each central unit including a plurality of memory interface ports;

a first memory subsystem including,

a buffer device, and

a memory bank coupled to the buffer device,

wherein data is transferred between the memory bank and the plurality of central units via the buffer device; and

a plurality of point-to-point links, each point-to-point link of the plurality of point-to-point links having a connection to a respective memory interface port of the plurality of central units, the plurality of point-to-point links including a first point-to-point link to connect the buffer device to a first memory interface port of the plurality of memory interface ports.

31. (New) The memory system of claim 30 further including:

a plurality of ports, wherein each port of the plurality of ports is connected to a respective point-to-point link of the plurality of point-to-point links; and

a plurality of memory subsystems, and wherein each memory subsystem of the plurality of memory subsystems includes:

a buffer device, wherein each of the buffers device is coupled to a respective port of the plurality of ports; and

a plurality of memory devices coupled to the buffer devices.

32. (New) The memory system of claim 31 further including a plurality of substrates wherein each memory subsystem of the plurality of memory subsystems is disposed on a respective substrate of the plurality of substrates.

33. (New) The memory system of claim 30 further including a plurality of sideband signals coupled between the plurality of memory devices of the first memory subsystem and the memory controller.

34. (New) The memory system of claim 30 further including a plurality of sideband signals coupled between the buffer device and the memory controller.

35. (New) The memory system of claim 30 further including a second memory subsystem including:

a buffer device, wherein the buffer device is connected to a second point-to-point link of the plurality of point-to-point links; and

a plurality of memory devices coupled to the buffer device.

36. (New) The memory system of claim 30 wherein each memory device of the plurality of memory devices included in the first memory subsystem includes a dynamic random access memory cell array.

37. (New) The memory system of claim 30 further including a module substrate having a port interface, wherein the first memory subsystem is disposed on the module substrate, and the buffer device is electrically connected to the port interface, wherein the

buffer device transceives data, control and address signals between the plurality of memory devices and the connector interface.

38. (New) The memory system of claim 30 wherein the buffer device further includes a cache memory configured to store data being provided from the memory controller to at least one memory device of the plurality of memory devices.

39. (New) The memory device of claim 30 wherein the buffer device further includes a write buffer configured to hold data to be provided to at least one memory device of the plurality of memory devices.

40. (New) A memory system comprising:

a controller device;

first and second buffer devices;

a first point-to-point link having a first connection to the controller device and a second connection to the first buffer device;

a first memory bank connected to the first buffer device;

a second point-to-point link having a first connection to the controller device and a second connection to the second buffer device; and

a second memory bank connected to the second buffer device.

41. (New) The memory system of claim 40, wherein the first buffer device and first plurality of memory devices are disposed on a first substrate, and the second buffer device and second plurality of memory devices are disposed on a second substrate.

42. (New) The memory system of claim 40 further including a third point-to-point link having a connection to the controller and a fourth point-to-point link having a connection to the controller.

43. (New) The memory system of claim 40 further including:

a first channel to connect the first plurality of memory devices to the second interface of the first buffer device;

a second channel to connect the second plurality of memory devices to the second interface of the second buffer device;

a third channel connected to the second interface of the first buffer device;

a third plurality of memory devices electrically coupled to the third channel;

a fourth channel connected to the second interface of the second buffer device; and

a fourth plurality of memory devices electrically coupled to the fourth channel.

44. (New) The memory system of claim 43 further including:

a fifth and sixth channel connected to the second interface of the first buffer device;

a fifth plurality of memory devices electrically coupled to the fifth channel; and

a sixth plurality of memory devices electrically coupled to the sixth channel.

45. (New) The memory system of claim 40 wherein each memory device of the first plurality of memory devices includes a dynamic random access memory cell array.

46. (New) The memory system of claim 40 further including a module substrate having a port interface, wherein the first buffer device is disaposed on the module substrate, and the first buffer device is electrically connected to the port interface, and wherein the first buffer device transceives data, control and address information between the first plurality of memory devices and the port interface.

47. (New) The memory system of claim 40 wherein the first buffer device further includes a cache memory, coupled to the first interface of the first buffer device, to store data being provided from the controller device to at least one memory device of the first plurality of memory devices.

48. (New) The memory device of claim 40 wherein the first buffer device further includes a write buffer, coupled to the first interface of the first buffer device, to hold data to be provided to at least one memory device of the first plurality of memory devices.

49. (New) A memory system comprising:

a controller device having an interface;

a first port, second port, and third port;

a first point-to point link having a first connection to the interface and a second connection to the first port;

a second point-to-point link having a first connection to the interface and a second connection to the second port;

a third point-to-point link having a first connection to the interface and a second connection to the third port; and

a first memory subsystem including:

a buffer device connected to the first port; and

a plurality of memory devices connected to buffer device, wherein at least one memory device of the plurality of memory devices transfer data to the controller device via the buffer device.

50. (New) The memory system of claim 49 wherein the second and third ports support coupling to respective second and third memory subsystems.

51. (New) The memory system of claim 49 wherein each memory device of the plurality of memory devices included in the first memory subsystem includes a dynamic random access memory cell array.

52. (New) The memory system of claim 49 further including a module substrate having a port interface, wherein the first memory subsystem is disposed on the module substrate, and the buffer device is electrically connected to the port interface, and wherein the buffer device transceives data, control and address signals between the plurality of memory devices and the connector interface.

53. (New) The memory system of claim 49 wherein the buffer device further includes a cache memory to store data being provided from the controller device to at least one memory device of the plurality of memory devices.

54. (New) The memory device of claim 49 wherein the buffer device further includes a write buffer to hold data to be provided to at least one memory device of the plurality of memory devices.

55. (New) A memory system comprising:

a memory controller having an interface that includes a plurality of memory subsystem ports;

a first memory subsystem including:

a buffer device having a first port and a second port, and

a plurality of memory devices coupled to the buffer device via the second port, wherein data is transferred between at least one memory device of the plurality of memory devices and the memory controller via the buffer device; and

a plurality of point-to-point links, each point-to-point link of the plurality of point-to-point links having a connection to a respective memory subsystem port of the plurality of memory subsystem ports, the plurality of point-to-point links including a first point-to-point link to connect the first port to a first memory subsystem port of the plurality of memory subsystem ports.

56. (New) The memory system of claim 55 further including:

a plurality of connectors, wherein each connector of the plurality of connectors is connected to a respective point-to-point link of the plurality of point-to-point links; and

a plurality of memory subsystems, and wherein each memory subsystem of the plurality of memory subsystems includes:

a buffer device having a first port and a second port, wherein the first port is coupled to a respective connector of the plurality of connectors; and

a plurality of memory devices coupled to the buffer device via the second port.

57. (New) The memory system of claim 55 further including a plurality of substrates wherein each memory subsystem of the plurality of memory subsystems is disposed on a respective substrate of the plurality of substrates.

58. (New) The memory system of claim 55 further including a plurality of sideband signals coupled between the plurality of memory devices of the first memory subsystem and the memory controller.

59. (New) A memory system comprising:

a controller device;

a first buffer device having a first interface and a second interface;

a second buffer device having a first interface and a second interface;

a first point-to-point link having a first connection to the controller device and a second connection to the first interface of the first buffer device;

a first plurality of memory devices connected to the second interface of the first buffer device;

a second point-to-point link having a first connection to the controller device and a second connection to the first interface of the second buffer device; and

a second plurality of memory devices connected to the second interface of the second buffer device.

60. (New) The memory system of claim 59, wherein the first buffer device and first plurality of memory devices are disposed on a first substrate, and the second buffer device and second plurality of memory devices are disposed on a second substrate.

61. (New) The memory system of claim 59 further including a third point-to-point link having a connection to the controller and a fourth point-to-point link having a connection to the controller.

62. (New) The memory system of claim 59 further including:

a first channel to connect the first plurality of memory devices to the second interface of the first buffer device;

a second channel to connect the second plurality of memory devices to the second interface of the second buffer device;

a third channel connected to the second interface of the first buffer device;

a third plurality of memory devices electrically coupled to the third channel;

a fourth channel connected to the second interface of the second buffer device; and

a fourth plurality of memory devices electrically coupled to the fourth channel.

63. (New) The memory system of claim 59 further including:

a fifth and sixth channel connected to the second interface of the first buffer device;

a fifth plurality of memory devices electrically coupled to the fifth channel; and

a sixth plurality of memory devices electrically coupled to the sixth channel.

64. (New) A memory system comprising:

a controller device having an interface;

a first connector, second connector, and third connector;

a first point-to point link having a first connection to the interface and a second connection to the first connector;

a second point-to-point link having a first connection to the interface and a second connection to the second connector;

a third point-to-point link having a first connection to the interface and a second connection to the third connector; and

a first memory subsystem including:

a buffer device connected to the first connector; and

a plurality of memory devices connected to buffer device, wherein at least one memory device of the plurality of memory devices transfer data to the controller device via the buffer device.

65. (New) The memory system of claim 64 wherein the second and third connectors support coupling to respective second and third memory subsystems.

66. (New) The memory system of claim 55 further including a second memory subsystem including:

a buffer device having a first port and a second port, wherein the first port is connected to a second point-to-point link of the plurality of point-to-point links; and

a plurality of memory devices coupled to the buffer device via the second port.

67. (New) The memory system of claim 55 wherein each memory device of the plurality of memory devices included in the first memory subsystem includes a dynamic random access memory cell array.

68. (New) The memory system of claim 55 further including a module substrate having a connector interface, wherein the first memory subsystem is disposed on the module substrate, and the buffer device is electrically connected to the connector interface, wherein the buffer device transceives data, control and address signals between the plurality of memory devices and the connector interface.

69. (New) The memory system of claim 68 further including a motherboard substrate having a socket which interfaces with the connector interface, wherein the memory controller and the plurality of point-to-point links are disposed on the motherboard substrate.

70. (New) The memory system of claim 55 wherein the buffer device further includes a cache memory coupled to the first port, to store data being provided from the memory controller to at least one memory device of the plurality of memory devices.

71. (New) The memory device of claim 55 wherein the buffer device further includes a write buffer, coupled to the first port, to hold data to be provided to at least one memory device of the plurality of memory devices.

72. (New) The memory system of claim 59 wherein each memory device of the first plurality of memory devices includes a dynamic random access memory cell array.

73. (New) The memory system of claim 59 further including a module substrate having a connector interface, wherein the first buffer device is disaposed on the module substrate, and the first buffer device is electrically connected to the connector interface, and wherein the first buffer device transceives data, control and address information between the first plurality of memory devices and the connector interface.

74. (New) The memory system of claim 64 wherein each memory device of the plurality of memory devices included in the first memory subsystem includes a dynamic random access memory cell array.

75. (New) The memory system of claim 64 further including a module substrate having a connector interface, wherein the first memory subsystem is disposed on the module substrate, and the buffer device is electrically connected to the connector interface, and wherein the buffer device transceives data, control and address signals between the plurality of memory devices and the connector interface.

76. (New) The memory system of claim 64 wherein the buffer device further includes a cache memory to store data being provided from the controller device to at least one memory device of the plurality of memory devices.

77. (New) The memory device of claim 64 wherein the buffer device further includes a write buffer to hold data to be provided to at least one memory device of the plurality of memory devices.